

# ***Evaluation Modules (EVMs) for TPS6012x and TPS6013x***

## *User's Guide*

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# Read This First

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### ***About This Manual***

The evaluation modules (EVMs) (TPS60120EVM-142 and TPS60130EVM-143) for the new Texas Instruments (TI™) charge pump devices TPS60120 and TPS60130 help designers to evaluate the devices. The TPS60120 and TPS60130 charge pumps (also called switched-capacitor dc/dc converters) are regulated, high efficiency dc/dc converter.

With these EVMs it is possible to evaluate the performance of the devices. Only a voltage source is needed to test the operation of the devices.

The layout of charge pumps is critical, similar to the layout of inductive dc/dc converters. Therefore, the layout given in this document is a good tool to reduce evaluation time for the designer.

### ***How to Use This Manual***

This document contains the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Schematic of the EVM

### ***Related Documentation From Texas Instruments***

Datasheet of TPS60120/TPS60121/TPS60122/TPS60123: Literature number SLVS257

Datasheet of TPS60130/TPS60131/TPS60132/TPS60133: Literature number SLVS258

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# Introduction

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The Texas Instruments (TI™) TPS60120 and TPS60130 charge pumps are regulated, high efficiency voltage converters. The TPS60120 delivers an output voltage of 3.3 V. The maximum output current is 200 mA for 2 V to 3.6 V, and 100 mA for 1.8 V to 2 V. The TPS60130 has an output voltage of 5 V. The maximum output current is 300 mA for an input voltage from 3 V to 5.4 V, and 150 mA for 2.7 V to 3 V.

Both devices work either as voltage doublers or, in 1.5-times mode, dependent on the input voltage. Therefore these devices are high efficiency charge pumps. For more details refer to the datasheets [literature numbers SLVS257 (TPS60120) and SLVS258 (TPS60130)].

The minimum number of external capacitors is four. The EVM is built with six (TPS60120) or five (TPS60130) external capacitors for optimized performance. Additional resistors and a capacitor at LBI and LBO are added. With the given resistor values, the LBO output delivers a low signal for an input voltage,  $V_{IN}$ , of 2 V or less for TPS60120, and 3 V or less for TPS60130. To select the resistor values for other input voltage ranges, refer to the datasheet.

The flying capacitors have to be ceramic because they are charged and discharged very fast and so their ESR has to be low. Tantalum capacitors are not able to handle such high frequencies, because the capacitance value of a tantalum capacitor decreases with increasing frequency.

The TPS60120 and TPS60130 EVM boards can also be used to evaluate other devices of this family (TPS60121, TPS60122, TPS60123, TPS60131, TPS60132, and TPS60133). For that purpose, replace the integrated circuit and capacitors C1 to C4 (see Chapter 2) with the values recommended in the datasheets. For devices with the powergood (PG) feature, the LBI resistors can be removed, but it is not necessary. The LBO pullup resistor works as the PG pullup; the LBO pad gives the PG signal.





# Schematic of the EVM

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The schematics of the two EVMs for TPS60120 and TPS60130 are the same. The differences between the boards are the IC itself and the values for the external components (see Tables 2–1 and 2–2),

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Figure 2–1. Schematic of the Evaluation Module (EVM)

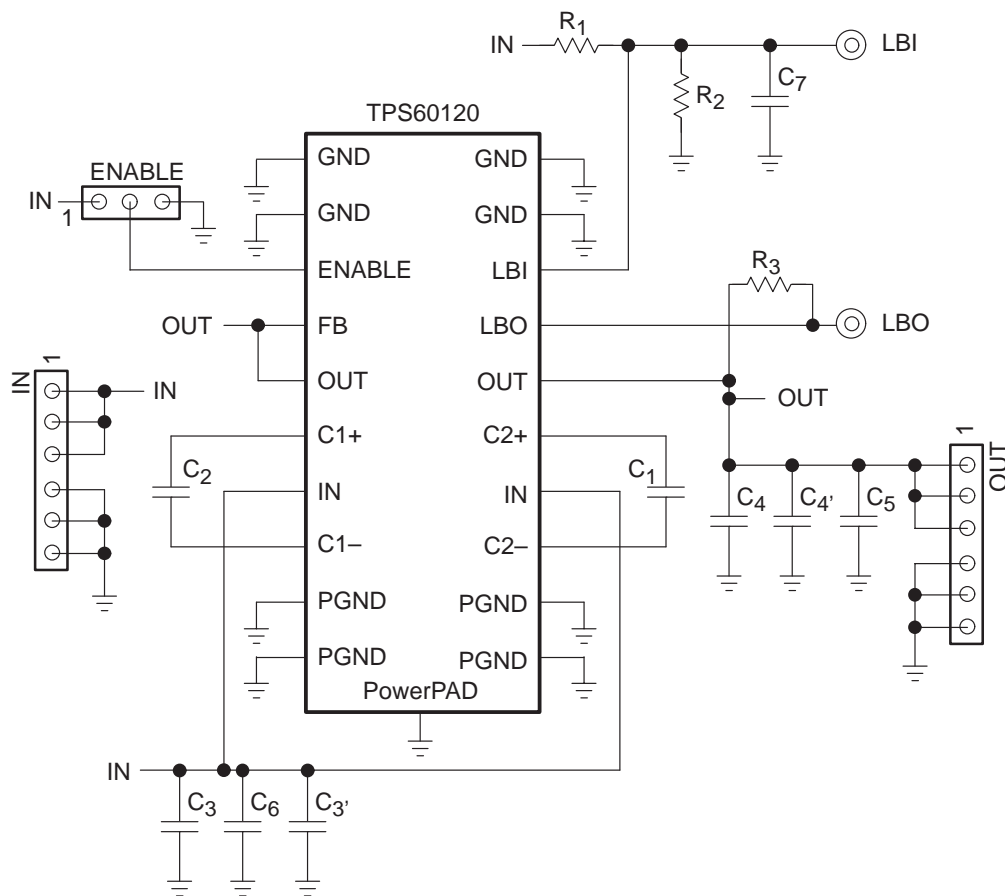


Table 2–1. Components on the TPS60120 EVM

Part	Value	Manufacturer, Part Number	Description
C1, C2	2.2 $\mu$ F, 10 V	Taiyo Yuden, LMK212BJ225MG-T	Ceramic flying capacitors
C3	10 $\mu$ F, 16 V	Sprague, 595D106X0016B2T	Tantalum input capacitor
C4	22 $\mu$ F, 10 V	Sprague, 595D226X0010B2T	Tantalum output capacitor
C5, C6	4.7 $\mu$ F, 10 V	Taiyo Yuden, LMK316BJ475KL-T	Ceramic bypass capacitors at input and output
C7	100 nF		Filter capacitor for the LBI input signal
R1	412 k $\Omega$	E96-Series	LBI input voltage adjustment
R2	634 k $\Omega$	E96-Series	LBI input voltage adjustment
R3	1 M $\Omega$		Pullup for the open drain output LBO

Table 2–2. Components on the TPS60130 EVM

Part	Value	Manufacturer, Part Number	Description
C1, C2	2.2 $\mu$ F, 10 V	Taiyo Yuden, LMK212BJ225MG-T	Ceramic flying capacitors
C3	10 $\mu$ F, 10 V	Taiyo Yuden, LMK325BJ106MN-T	Tantalum input capacitor
C4	33 $\mu$ F, 16 V	Sprague, 595D336X0016B2T	Tantalum output capacitor
C5	4.7 $\mu$ F, 10 V	Taiyo Yuden, LMK316BJ475KL-T	Ceramic bypass capacitors at input and output
C6			Empty
C7	100 nF		Filter capacitor for the LBI input signal
R1	590 k $\Omega$	E96-Series	LBI input voltage adjustment
R2	402 k $\Omega$	E96-Series	LBI input voltage adjustment
R3	1 M $\Omega$		Pullup for the open drain output LBO

Resistors R1/R2 adjust the input voltage of the LBI input for low battery detection. It is compared to the internal reference voltage of 1.21 V. Capacitor C7 works as a filter capacitor for the LBI input voltage. This capacitor is recommended because at the switching point of the LBI comparator, noise at the input can trigger the LBO and this can lead to oscillations at the LBO pin. Since the LBO output that signals a low battery state is an open drain output, it requires an external pullup resistor (R3). In applications that do not require low battery detection, these four parts can be omitted.

For the input and output voltages, there are two six-pin connectors on the board. Each has the first three pins for the supply (In or Out) and the last three pins for the ground (GND) signal.

The three-pin connector can be used to connect the ENABLE pin of the device. The connector has the supply (In) signal at the first pin, the logic signal at the second pin, and the ground (GND) signal at the third pin. This way it is possible to use jumpers to connect the pin either to input (supply voltage) or to ground to turn on or turn off the device. It is also possible to connect any other signal by using an external signal source and connecting it to the second pin. The ENABLE pin is a CMOS logic level input; refer to the data sheet for level specifications. The value of the signal connected to the logic pins can be higher than the supply voltage, but must not exceed the maximum ratings (see data sheet).

Applying a logic low level to the ENABLE input turns off the device and disconnects the output from the input. In this state, the supply current decreases to 0.05  $\mu$ A. For normal operation, connect the ENABLE signal to the input voltage or a logic high level respectively.

## 2.1 Layout of the EVM

Figure 2–1 and Figure 2–2 show the placement of the components and the layout of the EVM. The components and all signals are exclusively placed on the top layer of the PC board. To provide optimal performance, the bottom layer is a solid ground plane (only interrupted by some vias).

Figure 2–2. Placement of the Components

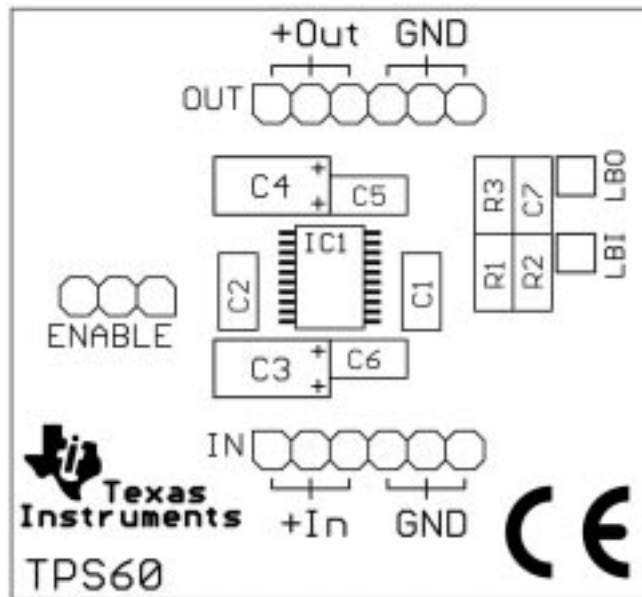


Figure 2–3. Top Layer of the EVM

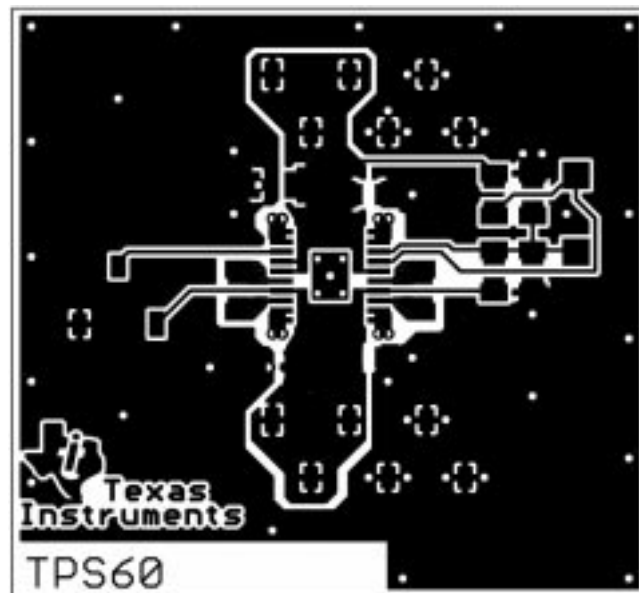


Table 2–1 and Table 2–2 contain the values and description of all capacitors and resistors that are placed on the EVM.

The space required for the IC and the capacitors on the EVM is approximately  $15 \text{ mm} \times 16 \text{ mm} = 240 \text{ mm}^2$

## 2.2 Setup of the EVM

For proper operation of the EVM, follow these steps:

- 1) Make sure that the ENABLE input is either properly jumpered or connected to an external source.
- 2) Connect a load to the output (between GND and Out)
  - TPS60120:  $> 16.5 \Omega$  or 0 mA to 200 mA ( $V_{IN}$  between 2 V and 3.6 V)  
 $> 33 \Omega$  or 0 mA to 100 mA ( $V_{IN}$  between 1.8 V and 2 V)
  - TPS60130:  $> 16.7 \Omega$  or 0 mA to 300 mA ( $V_{IN}$  between 3 V and 5.4 V)  
 $> 33.4 \Omega$  or 0 mA to 150 mA ( $V_{IN}$  between 2.7 V and 3 V)
- 3) Connect a dc power supply (or a battery pack) with an appropriate voltage between input (In), and ground (GND).
  - TPS60120: 1.8 V to 3.6 V
  - TPS60130: 2.7 V to 5.4 V

